What is claimed is:

1. An apparatus for verifying memory coherency of a duplication processor having a symmetrical structure comprising:

an active processor in which a standby memory read command (SMRC) is generated and transmitted by hardware and then a read data of the standby memory which has been inputted corresponding to the SMRC is image-buffered to verify a memory coherency; and

a standby processor in which the SMRC transmitted from the active processor is analyzed and a read command of a standby memory is outputted, and then the data read from the standby memory is transmitted to the active processor.

2. The apparatus according to claim 1, wherein the active processor comprising:

a standby memory image buffer (SMIB) for temporarily storing a read data of a standby memory;

a CPU for generating an SMRC;

a first memory controller for storing the read data of the standby memory in the SMIB;

a first processor bus controller for applying the read data of the standby memory to the first memory controller; and

a first duplication processor for informing the standby processor of a registered SMRC when the SMRC is registered by the CPU, and outputting a command done signal to the CPU when the reading operation of the standby

memory is completed.

3 The apparatus according to claim 1, wherein the SMRC includes a start address, the size of a data to be read and an address of an SMIB for storing a read data.

4. The apparatus according to claim 2, wherein the SMIB is provided in a predetermined region of the active memory.

5 The apparatus according to claim 2, wherein the first processor bus controller checks a transmission completion flag of each read data, and in case that the transmission completion flag has been set, the first processor bus controller outputs a write done signal to the first duplication processor.

6. The apparatus according to claim 2, wherein the first duplication processor generates a command done signal when it receives the write done signal from the first processor bus controller.

7 The apparatus according to claim 2, wherein when CPU receives the command completion signal from the first duplication processor, it compares the data of the active memory and the data of the SMIB to verify the memory coherency.

8. The apparatus according to claim 1, wherein the standby processor comprising:

a second memory controller for controlling access of the standby memory;

a second processor bus controller for transmitting a received SMRC to the second memory controller; and

a second duplication processor for analyzing the SMRC inputted through the second memory controller, sequentially generating a read address of the standby memory, and transmitting the data read from the standby memory to the active processor.

9 The apparatus according to claim 8, wherein the second duplication processor attaches an address of the SMIB included in the active processor to each read data.

10 The apparatus according to claim 8, wherein when the second duplication processor receives the final read data from the second memory controller, it sets a transmission completion flag of the corresponding read data.

11. A method for verifying memory coherency of a duplication processor comprising the steps of:

registering a standby memory read command (SMRC);

transmitting the registered SMRC to the standby processor;

analyzing the transmitted SMRC, reading the data of the standby memory and transmitting the read data to the active processor;

storing the read data as transmitted in the standby memory image buffer (SMIB); and

comparing the stored data of the SMIB and the stored data of the SMIB and verifying memory coherency.

12. The method according to claim 11, wherein the SMIB is provided in a predetermined region of the active memory.

13. The method according to claim 11, wherein the SMRC includes a start address, the size of a data to be read and an address of an SMIB for storing a read data.

14. The method according to claim 11, wherein the step of transmitting a read data comprising the sub-steps of:

analyzing the transmitted SMRC and sequentially generating a read address of the standby memory;

reading the data from the standby memory according to the generated address, and

checking whether the data has been read as much as requested and setting a transmission completion flag on the final read data.

15. The method according to claim 11, wherein the step of storing a read data comprising the sub-steps:

checking whether a transmission completion flag of the read memory has been set; and

storing a corresponding data in the SMIB according to the SMIB address in case that a transmission completion flag has not been set.

16 The method according to claim 15, further comprising the sub-

steps of:

generating a write done signal in case that a transmission completion flag of the read memory has been set; and

generating a command done signal when the write done signal is generated, and informing of completion of the operation of the SMRC.